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(54) **METHOD FOR OPERATING CMOS IMAGE SENSOR**

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a method for exactly operating a CMOS image sensor.
SOLUTION: A photodetector(PD) including matrixes of pixels (50) arranged in multiple lines and columns and each pixel stores electric charge carriers in proportion to illumination and storage means (C155) which can be connected with the photodetector(PD) at a given time to generate sampled signals to indicate the electric charge carriers stored by a photosensor are included. When the sampled signals stored in the storage means are readthe electric charge carriers generated by the photosensor are released and consequentlythe photodetector is held at voltage so that the sampled signals stored in the storage means are not disturbed. A diffusion problem of the electric charge to be typically generated regarding these sensors when they are operated by the conventional technology is solved by this invention.

CLAIMS

[Claim(s)]
[Claim 1]It is the method of operating a CMOS image sensor include a matrix of a pixel (50) arranged at two or more lines and sequencesEach of said pixel (50) contains optical sensor elements (PD) which accumulate an electric charge carrier proportional to Lighting Sub-Divisionand furtherin order to generate a sampled signal showing said electric charge carrier accumulated by said photosensor (PD)A storing means (C155) stored in order to be combined with said optical sensor elements (PD) at predetermined time and to read said sampled signal is includedWhen reading said said sampled signal which was stored in said storing means (C155)A method of operating a CMOS image sensorwherein said optical sensor elements (PD) are held at voltage which does not disturb said sampled signal which an electric charge carrier generated by said optical sensor elements (PD) was emittedtherefore was stored in said storing means (C1).
[Claim 2]Said optical sensor elements (PD) and said storing means (C155) are the 1st phase (A) or initialization phases which are initialized with predetermined initializing voltageSaid optical sensor elements (PD) and a phase when said storing means (C155) is separatedIn the 1st stage the 2nd phase (B) or an exposure phase which stores an electric charge carrier which said optical sensor elements (PD) were wide opened from said initializing voltageand is proportional to Lighting Sub-Divisionand said storing meansIt is wide opened from said initializing voltagenext is connected to said optical sensor elements (PD) between short time on the 2nd stageThereforein the 3rd phase (C) or a sampling phase which said sampled signal is generated and is stored in said storing means (C155)and the 1st stageIn [with said predetermined initializing voltagesaid optical sensor elements (PD) are initialized againnext] the 2nd stageA method according to claim 1 containing the 4th phase (D) or a reading phase when said sampled signal which was stored on said storing means (C155) is read.
[Claim 3]Each pixel (50) contains a reverse polarity photo-diode (PD) which constitutes said optical sensor elementsAnd the 1st2ndand 3rd MOS transistors (M1M2M3) are included at leastOn the other handsaid photo-diode (PD) is connected to the 1st power supply voltageandon the other handis connected to a source of said 1st and 2nd transistors (M1M2)A drain of said 1st and 3rd transistors (M1M3) is connected to the 2nd power supply voltageIt is connected mutuallyand a drain of said 2nd transistor (M2)

and said 3rd transistor (M3) form a memory node (55) of said storing means (C1)and it between said 1st phase (A)The 1st initializing signal (T1) and the 2nd initializing signal (RST) which are impressed to a gate of said 1st and 3rd transistors (M1M3) of each pixelrespectivelyIt is considered as said photo-diode (PD) and a level which initializes said memory node (55) with predetermined initializing voltageA control signal (SH) impressed to a gate of said 2nd transistor (M2) of each pixel is used as a level separated by said photo-diode (PD) and said memory node (55)and between said 2nd phase (B)Said photo-diode (PD) is wide opened from said initializing voltageand an electric charge carrier proportional to Lighting Sub-Division is used as a level to accumulate by said 1st initializing signal (T1)and it between said 3rd phase (C)In [said 2nd initializing signal (RST) is used as a level with which said memory node (55) is wide opened from said initializing voltage in the 1st stageand] the 2nd stageSaid photo-diode and said memory node are combined for said control signal (SH)Thereforea sampled signal is generatedand it is made a level stored on said memory node (55)and between said 4th phase (D)A method according to claim 2wherein said 1st initializing signal (T1) is used as a level which reinitialization of said photo-diode (PD) was carried out with said predetermined initializing voltageand was first stored on said memory node (55) and with which said sampled signal is read.

[Claim 4]Each pixel (50) contains the 4th and 5th MOS transistors (M4M5)A gatea drainand a source of said 4th transistor (M4)It is connected to a drain of said memory node (55)said 2nd power supply voltageand said 5th transistor (M5)respectivelyWhen a line selection signal (RSEL) is impressed to a gate of said 5th transistor (M5)a source of said 5th transistor (M5)Are a signal showing a sampled signal which exists on said memory node (55) the method of supplyingand between said 4th phase (D)A method according to claim 3 characterized by being addressed continuously in order to make it possible to read a sampled signal with which each line of a pixel exists on one memory node (55) of all the pixels of a line.

[Claim 5]Said 2nd initializing signal (RST) impressed to each 3rd transistor (M3) of said line of a pixel following each reading of a line of a pixel during said 4th phaseA signal which is used as a level that each memory node (55) of said line of a pixel is again initialized with said predetermined initializing voltageand exists then on each memory node (55) of a line of a pixel in front of

initialization and in the back. A method according to claim 4 using in order to generate a signal showing a difference between signals which exist on each memory node (55).
[Claim 6]A method according to any one of claims 3 to 5 which a photo-diode (PD) is formed by n type welland is characterized by said transistor (M1M3M1 and M5) being an n-MOS transistor.
[Claim 7]A method given in any 1 clause of said claimwherein said storing means (C1) comprises a capacitor protected from light by a metal layer.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention]Generally this invention relates to the method of operating an integration image sensor. This invention relates to the method of operating the integration image sensor which used the CMOS technologymore at details. Such a CMOS image sensor especially aims at manufacturing the photograph and video devices which were integrated.
[0002]
[Description of the Prior Art]As a result of the present integration technologyit is the integrated formand it is possible to manufacture an operational picture collecting device. The device has incorporated typically the processing constitution part which reads the data which realized the picture to be a photosensor formation part which comprises the assembly of the optical sensor elements systematized in the form of the matrixand was collected by the photosensor formation part after the same chip by such integration picture collection.
[0003]Traditionallyit depends for the integration picture collecting device on charge transfer technology. By such technologythe electric charge generated with light is a predetermined methodand is collected and transmitted. CCD (charge coupled devices) or CID (charge injection device) equipment is used for the charge transfer technology used most ordinarily. Although the device which uses these pieces of equipment has so far found out many commercial usesit still has a serious defect. It depends especially for these pieces of equipment on the production technology which is not a standardand the standard which does not have a Standard C MOS manufacturing process and compatibility in particular. Thereforesuch equipment becomes the hindrance

of integration of the whole image sensor at the expense of manufactureand the point of ease.
[0004]A certain concept was produced about using the p-n semiconductor junction usually called a photo-diode as optical sensor elements as what complements the above-mentioned technology. The essential advantage of such an element is perfect compatibility with a standard CMOS manufacturing process. Namelythe solution for which it depends on a photo-diode as optical sensor elementsConventional technologyOrl Yadid-Pecht especially included in this Description by referenceThe document of Ran Ginosar and Yosi Diamand "A Random Access Photodiode Arrayfor Intelligent Image Capture"It is publicly known from IEEETransactions on Electron DevicesVol.38no.8August 1991and pp1772-1780.
[0005]That isthis document is indicating the integration image sensor which used the CMOS technology in the form of a single chip. The same architecture of a sensor as a RAM memory is explained by drawing 1. Generallythis sensor shown with the reference number 1 includes the matrix 10 of the pixel arranged by M line and N sequence. This matrix 10 occupies the great portion of surface of a sensor. Reading of the specified pixel of the matrix 10 is performed by addressing a corresponding line and sequence. For this purposefurther both sensors include the output bus 30 combined with the sequence of the line address appointed circuit 20 combined with the matrix 10and the matrix 10 controlled by the control circuit 40.
[0006]Each pixel of the matrix 10 has the structure where it explains by drawing 2 A. Generallythis pixel shown with the reference number 50 of drawing 2 A contains optical-sensor-elements PDthe 1st stage A1the storing means C1and the 2nd stage A2. Optical-sensor-elements PD comprises the reverse polarity photo-diode which collects the electrons generated with light between integration periods. The 1st stage A1 is the sample and held type circuit which sample the value of the voltage which exists in both the terminals of photo-diode PD in predetermined time. Typicallythis sampled value is stored in the storing means C1 made with the capacitor. the pressure value stored in the capacitor C1 -- the transfer function of the 1st stage A1 -- and it is dependent on the ratio between the capacitance value of photo-diode PDand the capacitance value of the storing means C1 especially. The 2nd stage A2 reads the sampled voltage which was stored in the storing means C1. This structure where it is explained by drawing 2 A is read with detectionand enables separation of a process.

[0007]Various embodiments are assumed and shown in the above-mentioned document of conventional technology. Especially drawing 2 B shows one of the embodiments of these in which the pixel 50 contains reverse polarity (n type) photo-diode PD and five n-MOS transistors M1-M5. Each pixel 50 contains the memory node 55 which is made with a capacitor (capacitor C1)for exampleis protected from light by the protective metal layer.
[0008]TORAJISUTA M1 ensures initialization of photo-diode PD on predetermined voltage before each integration period. The transistor M2 samples the electric charge accumulated by photo-diode PDand stores the sampled signal in the memory node 55. This transistor M2 ensures an insulation or separation of photo-diode PD and the memory node 55. The transistor M3 ensures initialization of the memory node 55 on predetermined voltage. The transistor M4 is a source follower transistor. The transistor M5 is a line selection transistorand makes the voltage of the transistor M4 transmit certainly in a reading process to an output bus common to all the pixels of one sequence. The signal impressed to this structure contains high power-supply-voltage V_{DD} and low power source voltage V_{SS}.
A groundthe 1st initializing signal T1the sampling signal SHthe 2nd initializing signal RSTand the line selection signal RSEL are formed.

[0009]The 1st terminal of photo-diode PD is connected to ground $V_{SS}$and other terminals are connected to the source of the transistors M1 and M2 in which the gate was controlled by the signals T1 and SHrespectively. The drain of the transistor M1M3and M4 is connected to high power source voltage V_{DD}. The 2nd initializing signal RST is impressed to the gate of the transistor M3. Both the source of the transistor M3the drain of the transistor M2and the gate of the transistor M4 are connected to the pixel memory node 55. The source of the transistor M4 is connected to an output bus common to all the pixels of one sequence via the line selection transistor M5. The line selection signal RSEL is impressed to the gate of the transistor M5.
[0010]One problem produced about the structure of the pixel 50 where it is explained to drawing 2 Bin respect of performance exists in the fact which was stored on the memory node 55 and which is not no longer constant during the reading process. In factthe electric charge generated with light under photo-diode PD as described by the above-mentioned documentSince it being spread within a substrate and making the capacitor of the memory node 55 discharge

has time long enough in spite of protecting the node from lightyou are made to discharge the capacitance of the memory node 55 promptly in comparison. This electric charge carrier diffusion problem becomes increasingly more remarkable as the luminous intensity on the optical sensing area of a sensor becomes high. Thusit is understood that this diffusion phenomenon restricts rapidly the available time which makes possible reading of the sampled voltage which was stored on the pixel capacitor.
[0011]
[Problem to be solved by the invention]That isthis problem restricts the performance of a sensor. In order to obtain the snapshot of a dynamic scene especiallyit is desirable to perform overall exposure of a sensori.e.expose each pixel of a sensor matrix simultaneously. It will be made to be stored and to be unable to perform reading of the sampled voltage since voltage has actually changed with above-mentioned electric charge carrier diffusion phenomena considerably already between the time which reads the 1st line of a picture element matrixand the last line.
[0012]A glance target of this invention is proposing the method of operating the CMOS image sensor of the above-mentioned type which replies to the problem of the electric charge carrier diffusion produced about such a sensor.
[0013]Since other purposes of this invention have very short timeexposure time is proposing the method of operating the CMOS image sensor of the above-mentioned type which enables it to use this sensor for the application which is a decisive element.
[0014]Other purposes of this invention are to propose the method of operating the CMOS image sensor of the above-mentioned type of not requiring use of a mechanical shutter.
[0015]
[Means for solving problem]This invention is the method of operating the CMOS image sensor include the matrix of the pixel arranged at two or more lines and sequences. This method contains the optical sensor elements which accumulate the electric charge carrier with which each of a pixel is proportional to Lighting Sub-Divisionand furtherin order to generate the sampled signal showing the electric charge carrier accumulated by the photosensorAt predetermined timealso include the storing means combinable with optical sensor elementsand the storing meansWhen reading the sampled signal which is constituted so that it may store in order to read the sampled signaland was stored in the storing meansoptical sensor elementsIt is a method of operating a CMOS image sensor holding at voltage which

does not disturb the sampled signal which the electric charge carrier generated by the element was taken outtherefore was stored in the storing means.
[0016]Modification of the method by this invention forms the theme of a subordinate claim.
[0017]If the electric charge accumulated by the photo-diode during the integration period is sampled and one advantage of the method by this invention is stored in the storing capacitor which is each pixelit exists in the fact of making it photo-diode voltage turn into initializing voltage to the next collection promptly. As a resulteach optical generation electric charge is caughtor is emitted and does not diffuse the inside of a substrate to a memory node. In this waythe signal sampled on each pixel of a sensor maintains regularity. The reading process for every line of each pixel can happen by the conventional methodwithout requiring exposure time too much.
[0018]According to this inventionuse of an image sensor is attained in this way to the application in which exposure time is very short. A whole period required for exposure and processing of a picture is also reduced greatly. This is called a whole shutter.
[0019]Other advantages of this invention are on the fact that exposure and read operation are completely performed independently. Thusan electronic shutter is effectively operatedso that a mechanical shutter is not required any longer to operate a picture collecting device appropriately. Thereforethe manufacturing cost of those devices is also reduced.
[0020]In addition to other purposesfeaturesand advantagesthese purposesthe featureand an advantage of this invention will become clear by the following detailed explanation made with reference to an accompanying figure which was given by illustration which does not impose restriction.
[0021]
[Mode for carrying out the invention]A method by this invention operated to the pixel 50 of drawing 2 B is explained by drawing 3. Drawing 3 shows a time chart of generation of the control signal T1 which operates pixel structure of drawing 2 BSHRSTand RSEL. Generation of voltage V_{PD} of photo-diode PD and generation of voltage V_1 in the pixel memory node 55 are illustrated.
[0022]A method by this invention is not limited to operation of structure like structure where it was explained by drawing 2 BSince a sampled signal showing structurei.e.an electric charge carrier accumulated by

optical sensor elements during an integration periodwhere it was explained by drawing 2 A is generated and storedIt is applicable to a structure arbitrary type of taking a gross shape of structure include a storing means connected to the optical sensor elements at optical sensor elements and predetermined timesimilarly. Howeverstructure of drawing 2 B is simple and constitutes an advantageous structure especially.

[0023]It will be first recollected by the 1st that the 1st initializing signal T1 of the transistor M1 initializes photo-diode PD with predetermined initializing voltage before each integration period. The 1st initializing signal T1 is impressed to the whole sensor pixelnamelyphoto-diode PD of all the sensor pixels is simultaneously initialized by initializing voltage at the beginning of each integration period.

[0024]Similarlythe sampling signal SH is impressed to the whole sensor pixel so that photo-diode voltage may be simultaneously sampled and stored by the pixel memory node 55.

[0025]The 2nd initializing signal RST is impressed in either the whole or a line unit. Since the memory node of each pixel is initialized with predetermined initializing voltagethis 2nd initializing signal is first impressed to the wholeis a continuing phase and is impressed per line into a reading processso that it may see in detail below.

[0026]The line selection signal RSEL is impressed per line into a reading process.

[0027]The method by this invention can be divided at some continuation phases explained below. During the 1st phase A called an initialization phasesince the 1st and 2nd initializing signals T1 and RST initialize photo-diode PD and the memory node 55 of each pixel on predetermined voltageit both becomes high positive voltage.

[0028]Between this 1st phase Athe sampling signal SH serves as a low so that the transistor M2 may become non-conductiontherefore photo-diode PD and the memory node 55 may be separated. Similarlythe line selection signal RSEL is a low so that the line selection transistor M5 may become non-conduction.

[0029]Voltage V_{PD} of photo-diode PD ** and V_1 of the memory node 55 are set to a level about equal to predetermined initializing voltagerespectively.

[0030]Between the 2nd phase Bthe 1st initializing signal T1 changes to a low which makes the transistor M1 non-conduction. According to a light effectphoto-diode PD begins discharge in proportion to quantity of light which

each of photo-diode PD receivesas shown in a curve of voltage V_{PD} of drawing 3. It will be understood that exposure to light of a sensor starts by change of the initializing signal T1 from a high level to a low. This is the beginning of reset time.

[0031]During a whole period of the 2nd phase Bthe 2nd initializing signal RST is held on a level with which voltage of the memory node 55 of each pixel is held at constant value about equal to predetermined initializing voltage.

[0032]The 2nd initializing signal RST changes to a lowtherefore opens the memory node 55 in the end of the 2nd phase B. The 3rd phase C happens immediately after changing to a low from a high level of the initializing signal RST. Between this phaseit changes to a high level for a short timea pressure value of both ends of photo-diode PD passes the sampling transistor M2and the sampling signal SH is sampled and stored in the memory node 55. In this wayvoltage V_1 of the memory node 55 is generated as shown in drawing 3. In this waythe end of this 3rd phase C determines the end of exposure time of a sensor. The memory node 55 of each pixel actually stores a pressure value showing charge quantity generated under photo-diode PD during exposure of a sensor in this phase.

[0033]Immediately after a sampling signal changes to a lowthe 1st initializing signal T1 is used as a level with which each photo-diode is again initialized by voltage quite near initializing voltage. As a resultan electric charge generated by photo-diode is emitted by effect of light via the transistor M1. Thereforevoltage which sampled voltage which was stored in a memory node of each pixel of a sensor is no longer disturbed by electric charge carrier diffusion phenomenonand exists in this memory is maintained uniformly.

[0034]Thereforebetween the 4th phase D or a reading phaseeach pixel row of a sensor is continuously read without running a risk of a capacitor of a memory node being made to discharge by effect of an electric charge generated with light which will be diffused within a substrate. Between the 4th phaseeach line is continuously addressed so that each line may be read via an output bus of each sequence in sampled voltage which is each pixel. With setting to the 1st initialization phase Aa signal is impressed similarly and the next collection operation can begin in the end of this 4th phase.

[0035]As for this read operationfor a person skilled in the art known in the name of a correlation double sampling or

CDSperforming by publicly known technology is preferred. Operation which reads each line is separated into the 1st phase that reads voltage which exists in a memory node of a pixel of one lineand the 2nd reading phase when reinitialization of the memory node of a pixel of a line is carried out following the 1st phase by this publicly known technology. A signal which comprises a difference between sampled measured voltage and initializing voltage of a memory node is generated to each pixel. It becomes possible to remove a noise which exists in each pixel of a sensor according to few differences of sensitivity which may exist between fixed pattern noisesi.e.a pixelby this technology. As drawing 3 showsboth the line selection signal RSEL and the 2nd initializing signal RST are impressed per line between the 4th phase D in this way.

[0036]Thusit will be understood in the state where there is no risk of all the pixels being simultaneously exposed by this inventionand the sampled data receiving damage by an electric charge carrier diffusion phenomenon that reading is performed per line. Thereforethe CMOS image sensor operated by this invention operates like the camera which uses a mechanical shutter. In this waythe sampling transistor M2 achieves the function of an electronic shutter.

[0037]It is preferred that it is dependent on n well type photo-diodei.e.the photo-diode formed by n type wellby the improvement to an electric charge carrier diffusion phenomenon. This structure provides the advantage which forms the better barrier for diffusion of an electric charge carrier from the photodiode structure usually formedfor examplethe simple field of n type diffusion.

[0038]The correction and/or the improvement to this invention may be assumed without deviating from the range of this invention defined by the claim of the account of a head. Especially the pixel structure used by the example in order to explain the method by this invention could be theoretically manufactured including the additional transistorif it is complementary p-MOS technology or necessity. For exampleit will be understood that other composition can be provided in order to achieve that the sampling transistor M2 mainly has a role which separates a photo-diode and a memory nodeand this function.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1]It is an approximate account of the architecture of the already discussed conventional technology of a CMOS image sensor.
[Drawing 2 Adrawing 2 B] It is eachflow chartand detail view of a pixel of a publicly known structure. [of the already shown CMOS image sensor of drawing 1]
[Drawing 3]It is a time chart explaining the signal sequence applied to the pixel structure of drawing 2 B by this invention.
[Explanations of letters or numerals]
10 The matrix of a pixel
20 Line address appointed circuit
30 Output bus
40 Control circuit
50 Pixel
55 Memory node